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(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor: MOHINDRA, Rishi; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: VOLMER, Georg; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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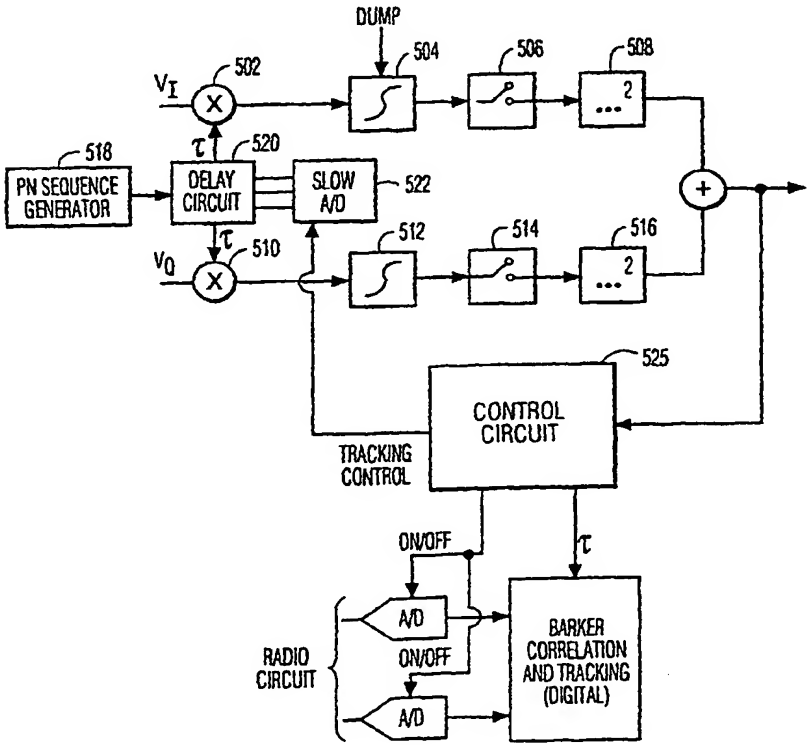
(54) Title: METHOD FOR EXTENDING DIGITAL RECEIVER SENSITIVITY USING ANALOG CORRELATION



(57) Abstract: Analog correlation techniques are used in a digital receiver portion of a spread spectrum transceiver to determine when to turn ON given digital receiver components. According to a particular embodiment, an analog correlator receives the down-converted in-phase and quadrature-phase outputs from the radio section and determines when a received signal is coming up at or near a given noise level. A control circuit is coupled to the correlator to selectively activate flash A/D converters in the digital receiver portion of the baseband processor. The analog correlator replaces the RSSI for "sniffing" whether a received signal is present.

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Method for extending digital receiver sensitivity using analog correlation

The present invention relates generally to the field of communication electronics and, in particular, to methods for extending the sensitivity of a digital receiver using analog correlation.

Spread spectrum is a communication technique that has found widespread use for both military and commercial applications. In a spread spectrum communication system, the transmitted modulation is spread (i.e., increased) in bandwidth prior to transmission over the channel and then despread (i.e., decreased) in bandwidth by the same amount at the receiver.

One of the target applications for spread spectrum is to facilitate wireless or radio communications between separated electronic devices. For example, a wireless local area network (WLAN) is a flexible data communication system that uses radio technology to transmit and receive data over the air, thereby reducing or minimizing the need for wired connections. In a typical WLAN, an access point is provided by a transceiver that connects a wired network from a fixed location. End users connect to the WLAN through transceivers that are typically implemented as PC cards in a laptop computer, or ISA or PCI cards for desktop computers. The transceiver may also be integrated with any device, such as a handheld computer, personal digital assistant, or the like.

The majority of the WLAN products available in the marketplace today are proprietary spread spectrum solutions targeting vertical applications operating in the 900MHz and 2.4GHz ISM frequency bands. These products include, as mentioned above, wireless adapters and access points in PCMCIA, ISA and custom PC board platforms. A typical spread spectrum transceiver comprises a conventional IF radio circuit, coupled to a baseband processor, which provides the desired modulation of the signal to be transmitted and the desired demodulation of a signal received at the transceiver. Thus, for example, the baseband processor may perform a given spread spectrum modulation technique such as direct sequence (DS) modulation, frequency hopping (FH) modulation, time hopping (TH) modulation, or hybrid modulations that blend together one or more of the various schemes.

In known spread spectrum transceivers that are designed to comply with the IEEE 802.11 WLAN Standard, the baseband processor typically includes on-board, dual parallel (or "flash") analog-to-digital (A/D) converters for processing the received I (in-phase) and Q (quadrature) signals from the quadrature IF demodulator in the radio section. Flash A/D converters perform the analog-to-digital conversion in one step, as opposed to a successive approximation. In particular, a flash A/D converter simultaneously compares the input analog voltage to 2^n - 1 threshold voltages to produce an n-bit digital code representing the analog voltage. Typically, the baseband processor also includes another flash A/D converter for converting the analog signal provided from a receive signal strength indicator (RSSI) in the radio section.

The RSSI, which gives an indication of the signal power, however, does not work efficiently for a low probability of false detection when the signal is at or near noise level (e.g., -95 dBm in an IEEE 802.11b receiver). In a typical inexpensive receiver (e.g., such as in an ISM 2.4 GHz system for IEEE 802.11b), the RSSI usually operates over the entire range of the input signal as illustrated in Figure 1. In a mid-range operation, it can be determined from the RSSI output signal that a received signal is coming up. In a noise-only situation, however, with V_{RSSI} at V min, the signal coming up cannot be detected unless it is about 10dB greater than the noise power so that the probability of false detection is low. This is also illustrated in Figure 1. Thus, the only way to determine with a low probability of false detection if the signal is at or near the noise level (i.e., when the RSSI is unreliable) is to do a separate correlation. This, in turn, requires that the flash A/D converters be maintained in an ON condition, even though those converters could be turned OFF following message transmission. Flash A/D converters draw large amounts of current and, as a result, exhibit large power consumption.

It would be desirable to increase the sensitivity of the receiver portion of a spread spectrum transceiver when the signal is coming up at or near noise level without having to first turn ON the flash A/D converters to "sniff" for the received signal. The present invention addresses this need.

Analog correlation techniques are used in a digital receiver portion of a spread spectrum transceiver to determine when to turn ON given digital receiver components when the received signal is coming up. According to a particular embodiment, an analog correlator receives the analog I and Q outputs from the radio section and attempts to lock a local

pseudorandom number (PN) sequence to a similar sequence in the received signal. When the analog correlator aligns the PN sequences, and if the corresponding correlation peak is sufficiently large, flash A/D converters in the digital receiver portion are turned ON. In effect, the analog correlator "sniffs" for the received signal because the radio signal strength indicator (RSSI) cannot detect received signal onset with a low probability of false alarm when the signal is at or near the noise floor.

In an illustrative embodiment, the analog correlator comprises, for each of the I and Q channels, an analog multiplier, an integrator and dump circuit, a sample-and-hold circuit, and an analog squarer. A pseudorandom (PN) sequence generator supplies a given PN sequence to each of the channels following the application of a selected delay. The PN sequence generator is the generator used to spread each data bit at a predetermined chip rate to supply the spread spectrum modulation. In a representative embodiment, the PN sequence is a Barker PN sequence. In operation, when the signal is at or near the noise level, following PN sequence lock, the correlator output is at a given relative correlation peak at the selected delay. When the given relative correlation peak exceeds a threshold, a control signal is output from the analog correlator to turn ON the flash A/D converters in the digital receiver. As a result, the large power-consuming flash A/D converters are only activated when the received signal is coming up and the relative correlation peak is above a given threshold. They need not be activated to sniff for the received signal, as in the prior art.

The foregoing has outlined some of the more pertinent objects and features of the present invention. These objects and features should be construed to be merely illustrative of some of the more prominent features and applications of the invention. Many other beneficial results can be attained by applying the disclosed invention in a different manner or modifying the invention as will be described. Accordingly, other objects and a fuller understanding of the invention may be had by referring to the following Detailed Description.

For a more complete understanding of the present invention and the advantages thereof, reference should be made to the following Detailed Description taken in connection with the accompanying drawings in which:

Figure 1 illustrates the relationship between the received signal strength indicator voltage and the signal strength in a conventional spread spectrum receiver;

Figure 2 is a block diagram of the architecture of a representative spread spectrum transceiver of the prior art;

Figure 3 is a block diagram of the components of the baseband processor of the spread spectrum transceiver of Figure 2;

Figure 4 is a block diagram of an analog correlator illustrating the basic operating principle of the present invention; and

Figure 5 is a more detailed block diagram illustrating how an analog correlator is used to control the digital receiver circuitry when the signal strength is at or near the noise level according to the present invention.

Figure 2 illustrates a known wireless transceiver 200 in which the present invention may be implemented. The transceiver may be used for WLAN applications in the 2.4 GHz ISM band in accordance with the proposed IEEE 802.11 standard, although this is not a limitation of the present invention. The transceiver comprises selectable antennas 202 coupled to a RF power amplifier and transmit/receive switch 204. A low noise amplifier 206 is also operatively coupled to the antennas. The transceiver also includes an up/down converter 208 connected to both the low noise amplifier 206 and the RF power amplifier and transmit/receive switch 204. The up/down converter 208 is connected to a dual frequency synthesizer 210 and a quadrature IF modulator/demodulator 212. IF modulator/demodulator 212 includes a received signal strength indicator (RSSI) function for providing an RSSI monitoring or "sniffing" function, as is well-known. One or more filters 214 and voltage controlled oscillators (VCOs) 216 may also be provided. The above components comprise a conventional radio portion of the spread spectrum transceiver. Familiarity with the operation of such components is presumed.

A spread spectrum baseband processor 218 is coupled to the radio portion and contains all of the functions necessary to facilitate full or half duplex packet-based spread spectrum communications as is also well-known in the art. In particular, the processor has on-board dual, flash A/D converters 220 and 222 for receiving in-phase (I) and quadrature (Q) signals from the IF modulator 212. The baseband processor also includes another A/D converter 224 for processing the received signal strength indicator (RSSI) voltage from the IF modulator 212. A clear channel assessment (CCA) circuit 226 provides a clear channel assessment function to avoid data collisions and to optimize network throughput. The flash A/D converter outputs are supplied to the demodulator 228, which despreads the received signal. The modulator 230 performs the spreading function, as is well understood. An interface circuit 232 is connected to the both the demodulator 228 and the modulator 230 to

interface the data to/from the baseband processor. Again, all of the above components are well-known to one of ordinary skill in the art.

One type of spread spectrum technique is direct sequence modulation. For illustration purposes, the present invention will be described in the context of a direct sequence baseband processor, although this is not a limitation of the invention as will be seen. A direct sequence modulation is formed by linearly modulating an output sequence of a pseudorandom number (PN) generator onto a train of pulses, each having a duration called the chip time. An 11 bit Barker sequence (i.e., +++---+--+-) may be used for this purpose. The use of an 11 bit Barker sequence, of course, is merely exemplary. A Barker sequence is a binary {-1,+1} sequence {s(t)} of length n having aperiodic autocorrelation values $|\rho_s(\tau)| < 1$ for all τ, $-(n-1) < \tau < n-1$. Typically, this type of modulation is used with binary phase-shift-keyed (BPSK) information signals. A direct sequence BPSK signal is generated by multiplying the BPSK signal by the direct sequence modulation. To demodulate a received BPSK signal, a local PN random generator (which generates the PN waveform at the receiver used for despreading) must be synchronized to within one chip of the PN waveform of the received BPSK signal. This function is done by a search routine that steps the local PN waveform sequentially in time by a fraction of a chip and, at each position, searches for a high degree of correlation between the received and local PN reference waveforms. The search ends when the correlation exceeds a given threshold, which is an indication that a coarse alignment has been achieved. After bringing the two PN waveforms into coarse alignment, a delay-locked or tau-dither tracking loop is used to maintain a fine alignment. Further details of this process are described, for example, in *The Communications Handbook*, 16.4 (1997), CRC Press, which is incorporated herein by reference.

Figure 3 illustrates the baseband processor 300 and its associated flash A/D converters 302 and 304. Theoretically, flash converters 302 and 304 could be turned OFF following the end of message (EOM) transmission (unless an acknowledgment is expected). In the prior art, however, this has not been practical. In particular, given the high probability of false alarm at the output when the signal is less than 10dB above the noise of the RSSI, it is not possible for the RSSI output to be used effectively to determine when the received signal strength is less than about 10 dB above the noise floor (about -95 dBm). Thus, in the prior art, the flash A/D converters must remain ON to "sniff" for the received signal onset near the noise floor (between about –95 and -85dBm). The flash A/D converters, which are required for that correlation, draw a large amount of current. To overcome this problem, and to reduce the overall power consumption of the digital receiver, the present invention extends

the digital receiver sensitivity by sniffing for the received signal with a low power analog correlator. When the analog correlator detects a correlation peak indicating the presence of the received signal, the flash A/D converters in the main baseband processor are turned ON. The components of the analog correlator are low power devices and, as a result of limiting the use of the flash A/D converters, the overall power consumption of the transceiver is significantly reduced as compared to the prior art.

Figure 4 illustrates the basic operation of the analog correlator 400. Generally, the analog correlator is used to synchronize a local PN sequence (e.g., an 11 bit Barker) to a similar PN sequence in the sampled down-converted in-phase and quad-phase signals V_I and V_Q. When the analog correlator aligns the PN sequence, and if the relative correlation peak is larger than a threshold, the flash A/D converters in the digital portion of the receiver section are turned ON. These converts are normally OFF following EOM transmission.

In this figure, only the in-phase (I) signal from the IF demodulator is shown as being processed. Of course, the correlator 400 includes a similar loop for processing the quadrature phase (Q) signal. As illustrated, the V_I signal from the IF demodulator stage is mixed in analog multiplier 402 with a Barker sequence generated by the 11 bit shift register 404 after that sequence is delayed, by delay circuit 406, by an amount τ. The 11 bit shift register operates at a given frequency, e.g., 11 MHz. The output of the analog mixer 402 is summed by sum circuit 408 and then sampled by sample circuit 410. The sample rate in this example is every 11 chips. The sampled output is then squared in squaring circuit 412 and added to the similarly-derived output for the Q signal, with the result supplied to a control circuit 414. In operation, the shift register output is synchronized to within one chip of the Barker waveform in the received V_I signal and the received V_Q signal. The control circuit then generates a signal to adjust the delay τ provided by the delay circuit 406 to maintain the Barker sequences in alignment. When the sequences are aligned the correlator has a given processing gain of, in the illustrated example, approximately 11. When the processing gain indicates a correlation peak above a given threshold, the received signal onset has occurred and the flash A/D converters are activated.

Figure 5 illustrates a preferred embodiment of the analog correlator 500 of the present invention for use in detecting the presence of the received signal when the signal is coming up at or near the noise floor. The correlator comprises an I channel branch including analog multiplier 502, integrator and dump circuit 504, sample and hold circuit 506 and analog squaring circuit 508. The Q channel branch comprises analog multiplier 510, integrator and dump circuit 512, sample and hold circuit 514 and analog squaring circuit 516.

Each branch is supplied with its respective V_I and V_Q signal together with the Barker (or other PN) sequence supplied from the PN generator 518. As in Figure 4, the PN sequence is delayed by a given amount τ by the delay circuit 520. The control circuit 525 generates a control signal that is converted to digital form by slow A/D converter 522 and used to control the delay circuit 520. A/D converter 522 and delay circuit 520 comprise a conventional tau-dither tracking loop. In operation, a peak correlation occurs when the PN sequences (from the PN generator and each respective I and Q signal) are within one chip. At this point, the control circuit 525 generates an output signal that is used by the tracking loop to set the delay τ so that the correlation remains at the peak value. When the correlation peak is above a given threshold, the control circuit 525 generates an output that activates the flash A/D converters 524 and 526 to an ON condition. As noted above, the converters 524 and 526 are normally OFF following an EDM transmission.

The control circuit may be implemented in any convenient manner, e.g. a software-driven processor, a microcontroller, a finite state machine, in handwired logic, an application-specific integrated (ASIC), a field programmable gave array (FPGA), a digital signal processor (DSP), or the like. Once the delay is determined, the control circuit may provide this value to the digital receiver to facilitate correlation by the digital components.

The analog correlator operates to detect when the received signal is coming up at or near the noise level (when the RSSI is otherwise ineffective). When a correlation peak occurs, the flash A/D converters are turned ON. This intelligent control of the flash A/D converters provides improved power management in the baseband processor and thus improved overall performance of the spread spectrum transceiver.

One of ordinary skill in the art will recognize that the analog correlation is of a relatively low quality from a signal detection point of view; on the contrary, the corresponding Barker correlation (performed in the digital receiver circuitry) provides a high quality signal detection. Thus, by way of generalization, the inventive technique utilizes an analog correlator for low quality signal detection and the normal digital correlator for high quality signal detection.

Having thus described my invention, what I claim as new is set forth in the following claims.

CLAIMS:

1. In a spread spectrum transceiver (200) comprising a radio circuit (208, 212) coupled to a baseband processor (218), the baseband processor including a spread spectrum despreader and flash A/D converters (220, 222) for sampling down-converted in-phase and quadrature-phase signals received from the radio circuit, the improvement comprising:

an analog correlator (400) for detecting when a received signal is coming up at or near a given noise level; and

a control circuit (414) coupled to the analog correlator for selectively activating the flash A/D converters.

2. In the spread spectrum transceiver as described in Claim 1 wherein the analog correlator comprises a pseudorandom number (PN) sequence generator (518), an in-phase section, and a quadrature phase section.

3. In the spread spectrum transceiver as described in Claim 2 wherein the in-phase section comprises:

an analog multiplier (502) for receiving the down-converted in-phase signal from the radio circuit and a bit sequence generated by the PN sequence generator and, in response thereto, generating a first signal;

an integrator and dump circuit (504) for integrating the first signal over a given time period to generate a second signal;

a sample and hold circuit (506) for sampling the second signal and generating a third signal; and

an analog squaring circuit (508) for squaring the third signal and generating a fourth signal.

4. In the spread spectrum transceiver as described in Claim 2 wherein the quadrature phase section comprises:

an analog multiplier (510) for receiving the down-converted quadrature-phase signal from the radio circuit and a bit sequence generated by the PN sequence generator and, in response thereto, generating a first signal;

an integrator and dump circuit (512) for integrating the first signal over a given time period to generate a second signal;

a sample and hold circuit (514) for sampling the second signal and generating a third signal; and

an analog squaring circuit (516) for squaring the third signal and generating a fourth signal.

5. In the spread spectrum transceiver as described in Claim 2 wherein the PN sequence generator generates a Barker sequence.

6. In the spread spectrum transceiver as described in Claim 5 wherein the Barker sequence is an 11 bit Barker.

7. In the spread spectrum transceiver as described in Claim 2, further including:

a tracking loop (522, 520) for maintaining a PN sequence output from the PN sequence generator in alignment with a PN sequence in the down-converted in-phase and quadrature-phase signals received from the radio circuit.

8. A transceiver, comprising:

a radio circuit (208, 212);

a baseband processor (218) coupled to the radio circuit and including a demodulator and A/D converters for sampling down-converted in-phase and quadrature-phase signals received from the radio circuit;

a PN sequence generator (404);

an analog correlator (400) for detecting when a received signal is coming up at or near a given noise level;

a tracking loop (406) for maintaining a PN sequence output from the PN sequence generator in alignment with a PN sequence in the down-converted in-phase and quadrature-phase signals received from the radio circuit following detection of the received signal; and

a control circuit (414) coupled to the analog correlator for selectively switching the flash A/D converters from an OFF condition to an ON condition.

9. A spread spectrum transceiver for use in a wireless local area network (WLAN), comprising:

a radio circuit (208, 212) ;

a baseband processor (218) coupled to the radio circuit and including a spread spectrum despreader and digital circuitry for high quality signal detection;

an analog correlator (400) for sniffing for a received signal; and

circuitry (414) coupled to the analog correlator for selectively activating the digital circuitry to enable high quality signal detection.

10. A method for extending the sensitivity of a digital receiver having a radio circuit (208, 212), and a baseband processor (218) coupled to the radio circuit, comprising:

while given digital receiver components are turned off, performing an analog correlation (400) to detect when a received signal is coming up at or near a given noise level; and

when the received signal is detected, switching on (414) the given digital receiver components.

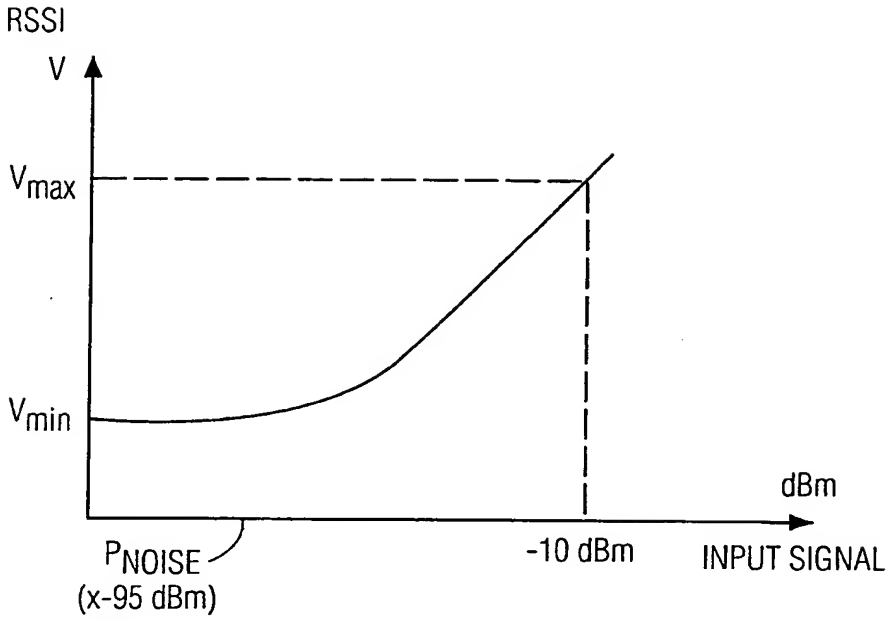


FIG. 1

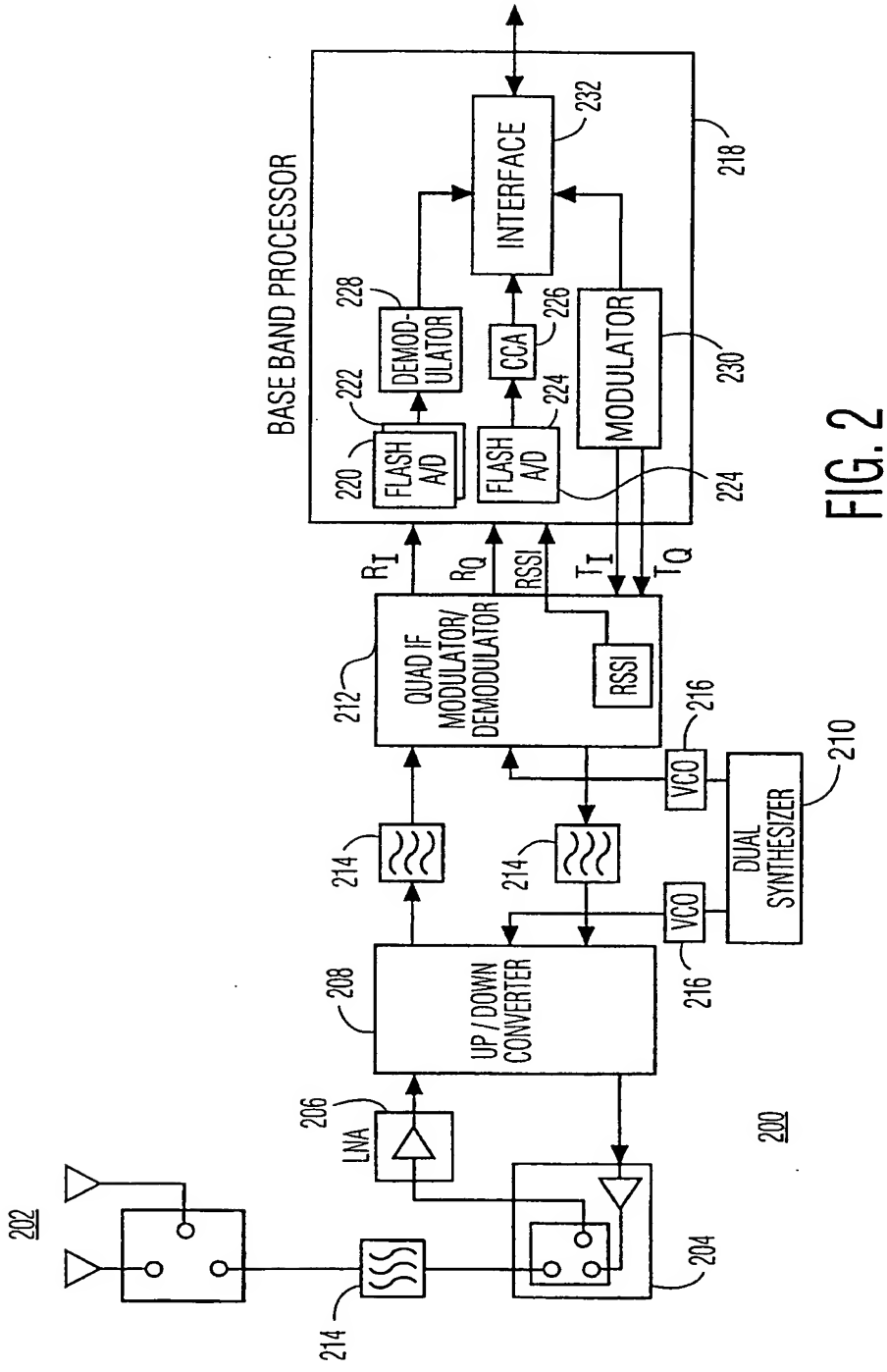

BASE BAND PROCESSOR
INTERFACE
232
218
228
DEMOD-ULATOR
226
CCA
230
MODULATOR
222
224
220
FLASH A/D
FLASH A/D
224
RI
RQ
RSSI
TI
TQ
212
QUAD IF MODULATOR/ DEMODULATOR
RSSI
216
VCO
210
DUAL SYNTHESIZER
214
214
VCO
216
208
UP / DOWN CONVERTER
206
LNA
200
202
214
204

FIG. 2

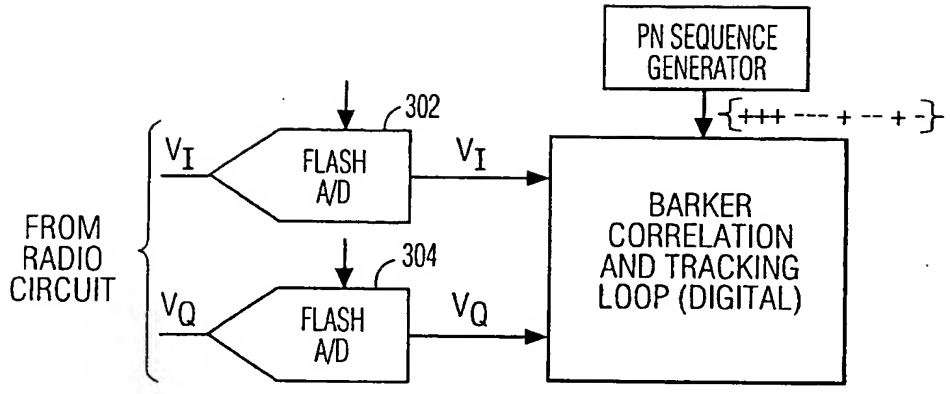

PN SEQUENCE GENERATOR
{+++ --- + -- + -}
302
V_I
FLASH A/D
V_I
FROM RADIO CIRCUIT
304
V_Q
FLASH A/D
V_Q
BARKER CORRELATION AND TRACKING LOOP (DIGITAL)

FIG. 3

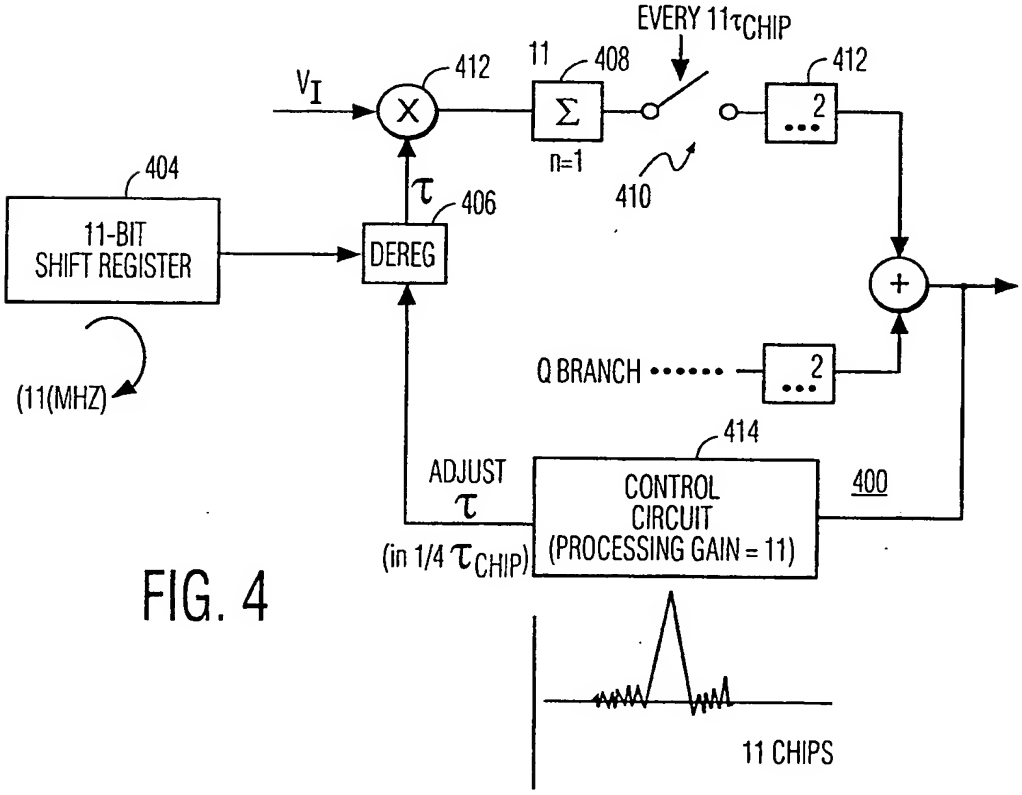
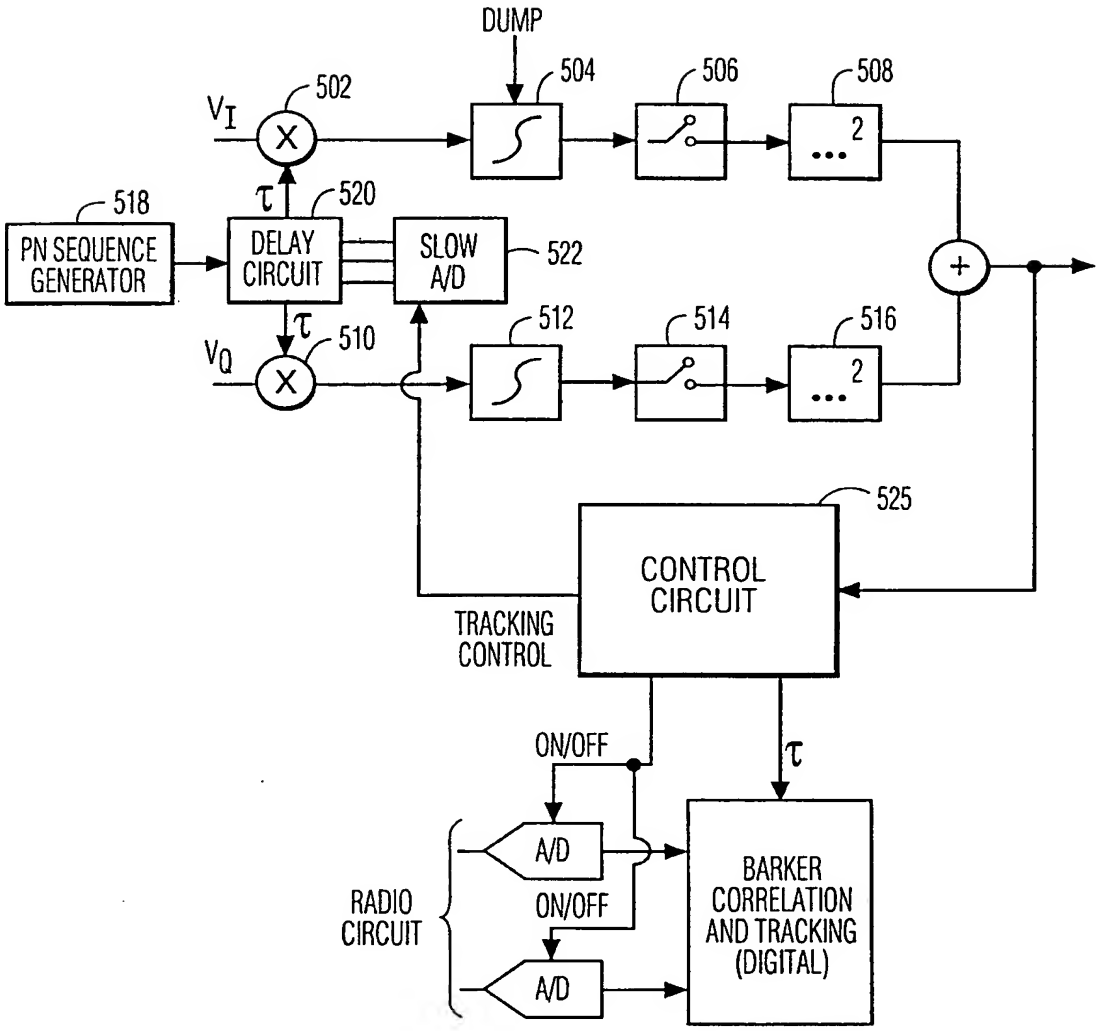

EVERY 11τ_{CHIP}
V_I
412
11
408
412
X
Σ
n=1
2
410
404
τ
406
11-BIT SHIFT REGISTER
DEREG
+
Q BRANCH
2
(11(MHZ)
414
ADJUST τ
(in 1/4 τ_{CHIP})
CONTROL CIRCUIT (PROCESSING GAIN = 11)
400
11 CHIPS

FIG. 4


DUMP
502
504
506
508
V_I
X
2
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520
τ
PN SEQUENCE GENERATOR
DELAY CIRCUIT
SLOW A/D
522
+
τ
510
512
514
516
V_Q
X
2
525
CONTROL CIRCUIT
TRACKING CONTROL
ON/OFF
τ
A/D
RADIO CIRCUIT
ON/OFF
BARKER CORRELATION AND TRACKING (DIGITAL)
A/D

FIG. 5

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/EP 00/11396

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/16 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 96 14697 A (STRUHSAKER PAUL F ;SMITH JANE L (US); AERONET WIRELESS COMMUNICATI) 17 May 1996 (1996-05-17) abstract; figure 1	1-10
A	US 5 598 429 A (MARSHALL KENNETH E) 28 January 1997 (1997-01-28) abstract; figure 5	1-10
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 12, 29 October 1999 (1999-10-29) & JP 11 177524 A (HITACHI LTD;HITACHI MEDIA ELECTORONICS CO LTD), 2 July 1999 (1999-07-02) abstract	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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°O° document referring to an oral disclosure, use, exhibition or other means

°P° document published prior to the international filing date but later than the priority date claimed

°T° later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

°X° document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

°Y° document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

°&° document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 2001	20/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Kolbe, W

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int :ional Application No
PCT/EP 00/11396

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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